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Amendment to the Specification

The Paragraph beginning at Page 3, line 16, is to be amended as follows:

Fig. 16 is impedance diagram for the transistors of the CMOS inverter of Fig. 15.; and Fig. 17 is a block diagram illustrating relative positioning of regular and non-flashing CMOS components.

The Paragraph beginning at Page 108, lines 7-14, is to be amended as follows:

Finally, regular CMOS inverters can be positioned near critical non-Flashing CMOS components. These inverters should take their input signal from the Tamper Detection Line above. Since the Tamper Detection Line operates multiple times faster than the regular operating circuitry, the net effect will be a high rate of light-bursts next to each non-Flashing CMOS component. Since a bright light overwhelms observation of a nearby faint light, an observer will not be able to detect what switching operations are occurring in the chip proper. This arrangement is conceptually illustrated in Figure 17 with the noise generator 121, tamper detection line 120, regular CMOS inverter 130 and non-flashing CMOS component 150. These regular CMOS inverters will also effectively increase the amount of circuit noise, reducing the SNR and obscuring useful EMI.